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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/875,501
Filing Date . . . . . June 4, 2001
Inventor . . . . . Klaus F. Schuegraf, et al.
Assignee . . . . . Micron Technology, Inc.
Group Art Unit 2815
Examiner . . . . . E. Ortiz
Attorney's Docket No. MI22-1741
Title: Methods for Forming Wordlines, Transistor Gates, and Conductive Interconnects, and Wordline, Transistor Gate, and Conductive Interconnect

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

The Examiner's attention is directed to the references which are listed on the attached Form PTO-1449, a copy of which is attached. No admission is made regarding whether all the submitted references are prior art.

Citation of these references is respectfully requested.

Respectfully submitted,

Dated: 12-12-03 By: _____
D. Brent Kenady
Reg. No. 40,045

Form PTO-1449 | U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

LIST OF ART CITED BY APPLICANT

(Use several sheets if necessary)

ATTY. DOCKET NO.	SERIAL NO.
MI22-1741	09/875,501
APPLICANT: Klaus Florian Schuegraf et al.	
FILING DATE: 06/04/01	GROUP: 2815

U.S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

	AC		Ohnishi, K. et al., *Improving Gate Oxide Integrity (GOI) of a W/Wnx/dual-poly Si Stacked-Gate by Using Wet-Hydrogen Oxidation in 0.14-μm CMOS Devices*, IEEE. 1998. pgs. 397-400.
	AD		Kawada, K. et al., *Water Vapor Generator By Catalytic Reactor*, pgs. 10-16.
	AE		Wakabayashi, H. et al., *An Ultra-Low Resistance and Therma Stable W/pn-Poly-Si Gate CMOS Technology using Si/TiN Buffer Layer*, IEEE. 1998. pgs. 393-396.
	AF		Hiura, Y. et al., *Integration Technorology of Polymetal (W/WSiN/Poly-Si) Dual Gate CMOS for 1 Gbit DRAMs and Beyond*, IEEE. 1998. pgs. 389-392.
	AG		Nagahama, T. et al., *Wet Hydrogen Oxidation System for Metal Gate LSI's*, pgs. 140-143
	AH		Lee, B. et al., *In-situ Barrier Formation for High Reliable W/barrier/poly-Si Gate Using Denudation of WN_x on Polycrystalline Si*, IEEE. 1998 pgs. 385-389.

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.